IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 7-15 and 20-30 without prejudice or disclaimer, AMEND claims 1, 16, 31, and 33, and ADD new claims 34-40 in accordance with the following:

1. (CURRENTLY AMENDED) A thin film transistor, comprising:

an active layer formed on an insulating substrate and having channel, source, and drain regions formed therein;

wherein a voltage is applied to the channel region to discharge hot carriers generated in the channel region and the channel region is an intrinsic region.

2. (ORIGINAL) The thin film transistor according to claim 1, wherein the voltage applied to the channel region is equal to a voltage applied to the source or drain region.

3. (ORIGINAL) The thin film transistor according to claim 1, wherein the active layer further comprises a bias supply layer contacted with the channel region and separated from the source and drain regions, wherein the voltage applied to the channel region is directly applied to the bias supply layer.

4. (ORIGINAL) The thin film transistor according to claim 3, wherein a conductivity type of the bias supply layer is different from a conductivity type of the source and drain regions, and the voltage applied to the bias supply layer is equal to a voltage applied to the source or drain region.

5. (ORIGINAL) The thin film transistor according to claim 1, wherein the active layer further comprises:

a bias supply layer contacted with the channel region and separated from the source and drain regions; and

a contact wiring connected to the bias supply layer to apply the voltage to the channel

region through the bias supply layer,

wherein the voltage applied to the channel region is directly applied to the bias supply layer through the contact wiring.

6. (ORIGINAL) The thin film transistor according to claim 5, wherein a conductivity type of the bias supply layer is different from a conductivity type of the source and drain regions, and the voltage applied to the bias supply layer is equal to a voltage applied to the source or drain region.

7-15. (CANCELED).

16. (CURRENTLY AMENDED) A flat panel display comprising:

a gate line, a data line and a power supply line; and

a plurality of pixels connected to the lines;

wherein each of the pixels comprises one or more thin film transistors comprising channel, source, and drain regions in an active layer, and a voltage is applied to the channel region of the thin film transistor to discharge hot carriers, and the channel region is an intrinsic region.

17. (ORIGINAL) The flat panel display according to claim 16, wherein the thin film transistor further comprises:

a bias supply layer formed in the active layer so that the bias supply layer is contacted with the channel region and separated from the source and drain regions; and

a contact wiring connected to the bias supply layer to apply the voltage to the channel region.

18. (ORIGINAL) The flat panel display according to claim 16, wherein a conductivity type of the bias supply layer is different from a conductivity type of the source and drain regions.

19. (ORIGINAL) The flat panel display according to claim 17, wherein the bias supply layer is connected to the data line or power supply line though the contact wiring.

20-30. (CANCELED).

31. (CURRENTLY AMENDED) An active layer of a thin film transistor, the active layer comprising:

a source region;

a drain region;

a channel region; and

a bias supply region to supply a voltage to the channel region to discharge hot carriers wherein the channel region is an intrinsic region.

32. (ORIGINAL) The active layer of claim 31, wherein the bias supply region is connected to the source or drain region.

33. (CURRENTLY AMENDED) A thin film transistor, wherein a voltage is applied to a channel region by a member other than a gate electrode, and wherein the voltage discharges hot carriers generated in the channel region, and the channel region is an intrinsic region.

34. (NEW) The thin film transistor of claim 3, wherein the bias supply layer is in direct contact with the channel region at a position that is perpendicular to and in between the source and drain regions.

35. (NEW) The flat panel display of claim 17, wherein the bias supply layer is in direct contact with the channel region at a position that is perpendicular to and in between the source and drain regions.

36. (NEW) The active layer of the thin film transistor of claim 31, wherein a bias supply region is in direct contact with the channel region at a position that is perpendicular to and in between the source and drain regions.

37. (NEW) A flat panel display, comprising:

a gate line, a data line and a power supply line; and

a plurality of pixels connected to the lines,

wherein each of the pixels comprises first and second thin film transistors each comprising a bias supply layer, a channel region, a source region, and a drain region in an active layer; and voltage is applied to the channel regions of the thin film transistors to discharge hot

carriers; and the source, channel, and drain regions of each of the thin film transistors extend parallel to the gate line, and the channel region and the bias supply layer of each of the thin film transistors extend parallel to the data or power supply lines.

38. (NEW) The flat panel display of claim 37, wherein the bias supply layer and the source region of the first thin film transistor are connected to the data line.

39. (NEW) The flat panel display of claim 37, wherein the bias supply layer and the source region of the second thin film transistor are connected to the power supply line.

40. (NEW) The flat panel display of claim 37, further comprising a capacitor having a first electrode and a second electrode, and the second thin film transistor comprising a gate electrode, wherein the drain region of the first thin film transistor and the gate electrode of the second thin film transistor are connected to the first electrode of the capacitor, and the second electrode of the capacitor is connected to the power supply line.